Fig. 1

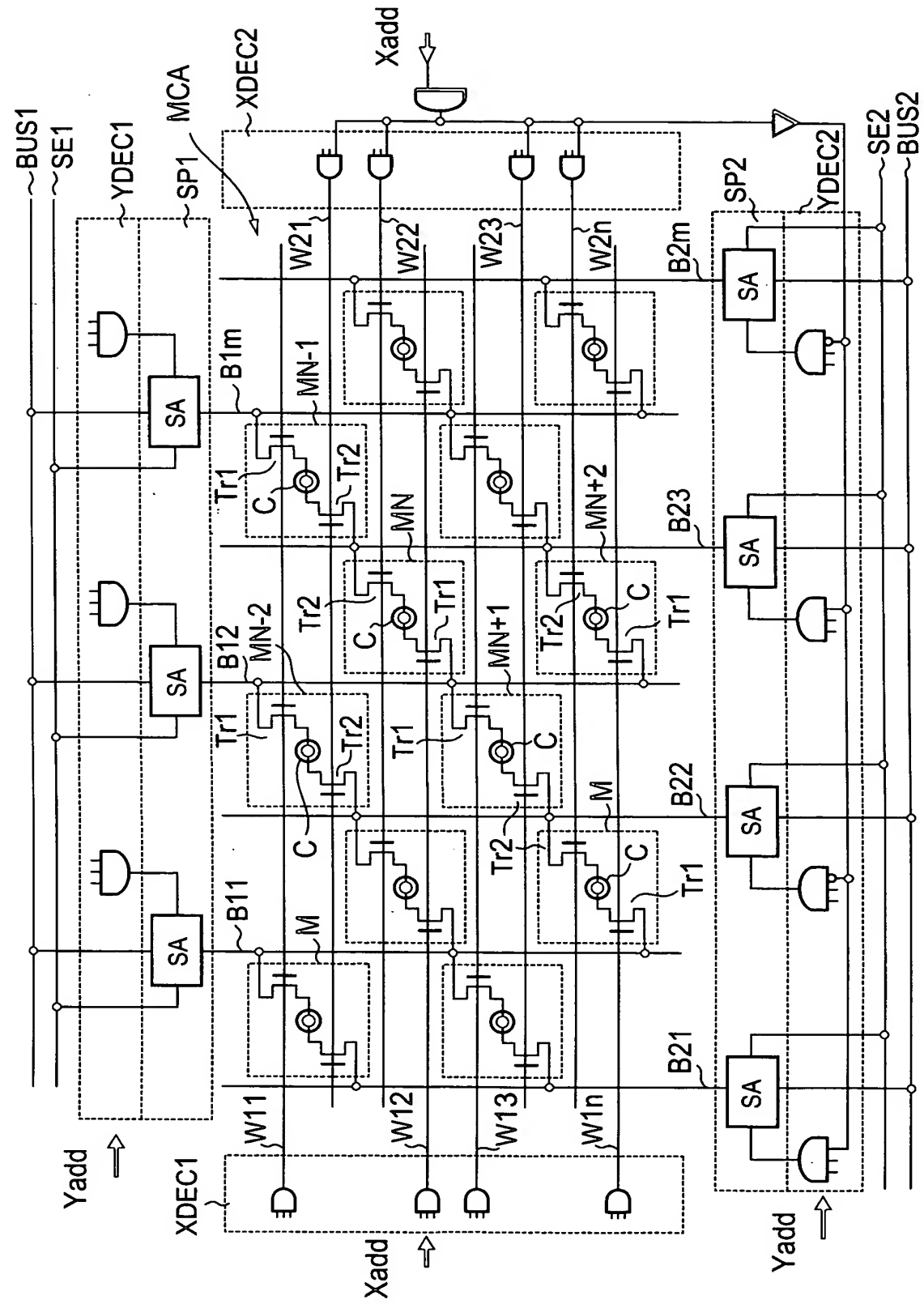

BUS1
SE1
YDEC1
MCA
SP1
XDEC2
Xadd
SE2
BUS2
YDEC2
SP2
SA
B1m
B12
B11
B2m
B23
B22
B21
W21
W22
W23
W2n
W11
W12
W13
W1n
MN-1
MN
MN-2
MN+1
MN+2
M
Tr1
Tr2
C
Yadd
XDEC1
Xadd
Yadd

Fig. 2

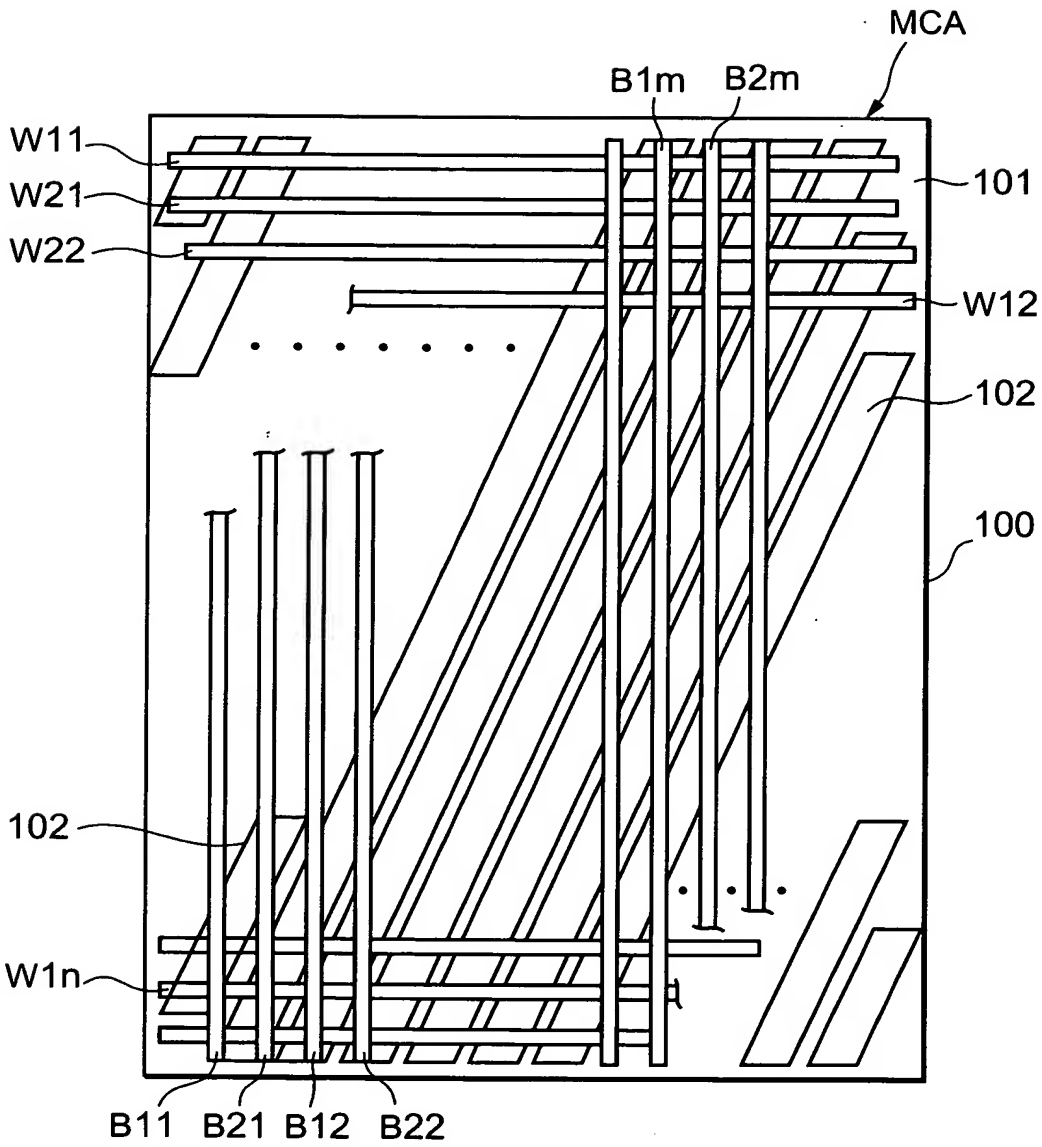


Fig. 3

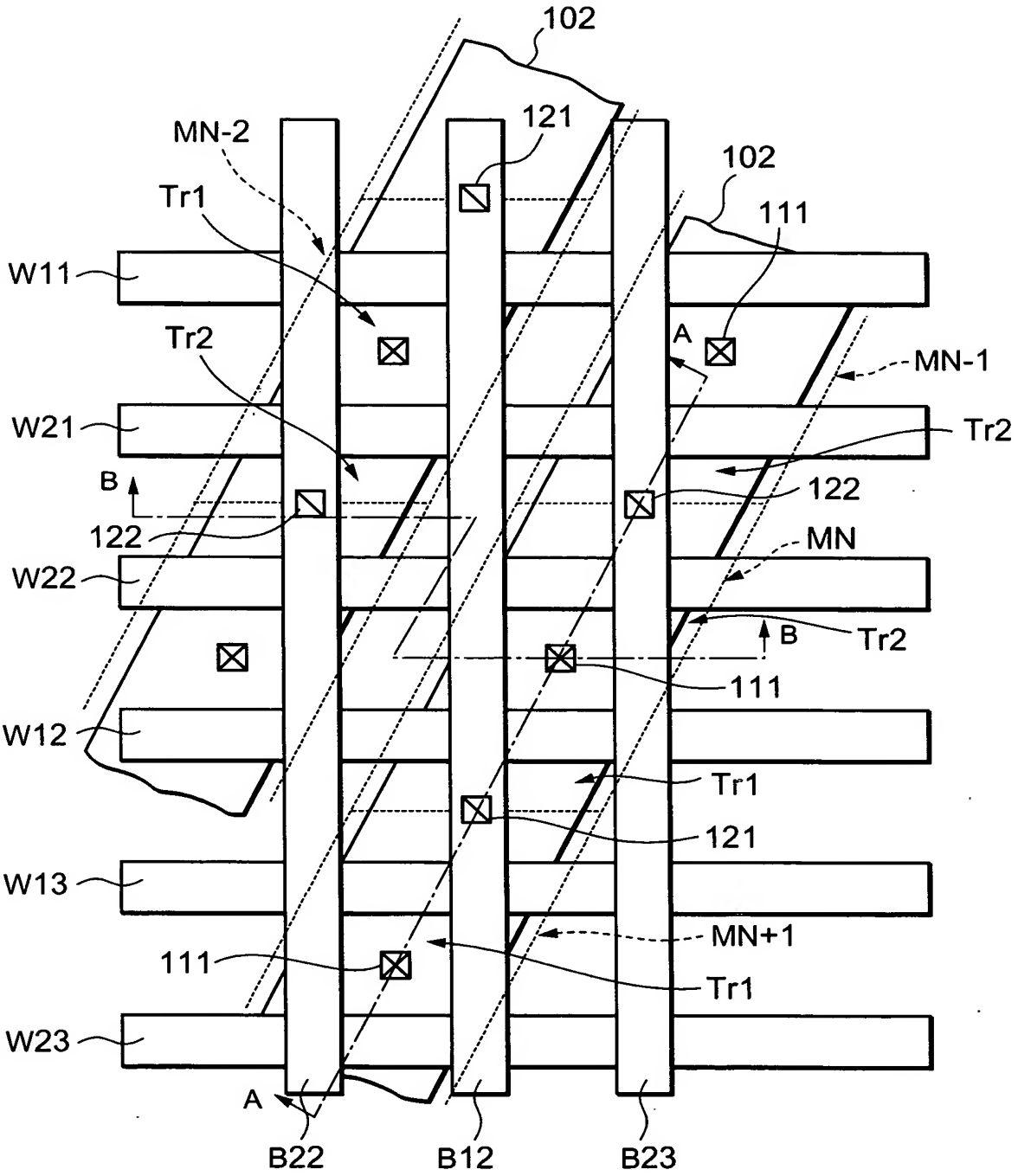

102
MN-2
121
102
Tr1
111
W11
Tr2
A
MN-1
W21
Tr2
B
122
122
MN
W22
B
Tr2
111
W12
Tr1
121
W13
MN+1
111
Tr1
W23
A
B22
B12
B23

Fig. 4

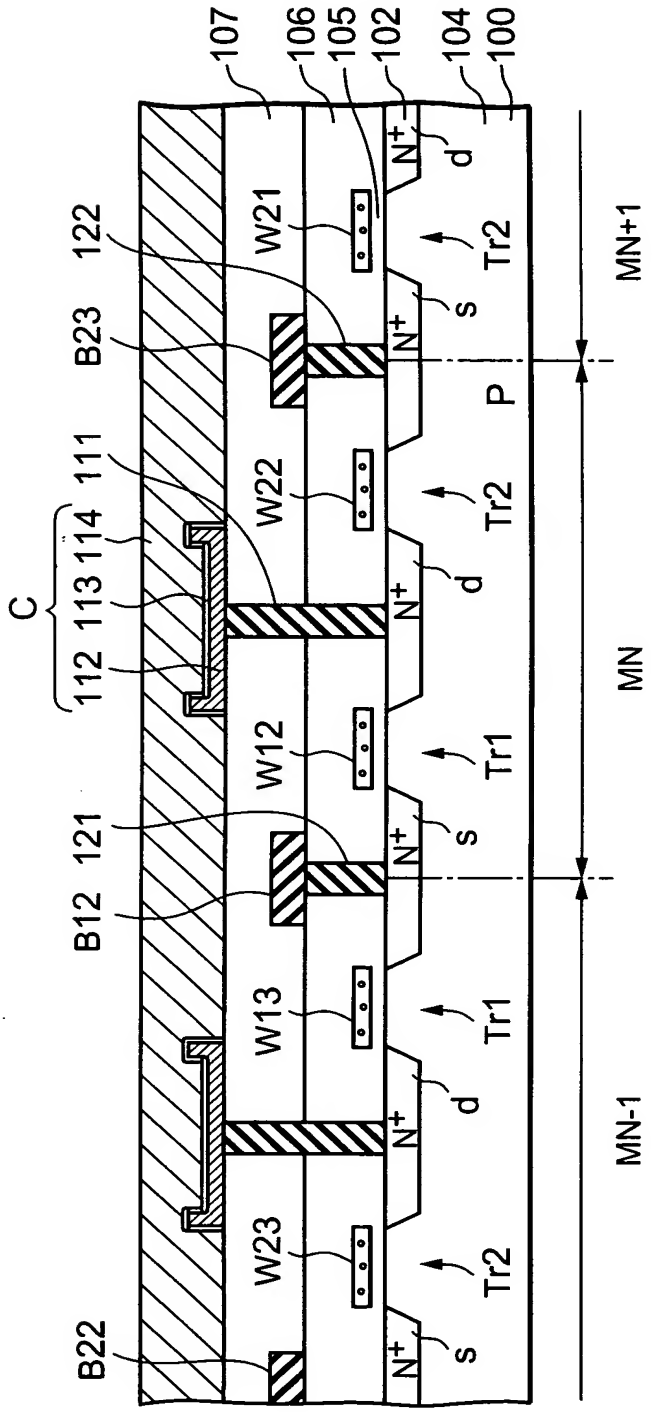

107
106
105
102
104
100
122
B23
111
C
114
113
112
121
B12
B22
W21
W22
W12
W13
W23
Tr2
Tr1
N+
d
s
P
MN+1
MN
MN-1

Fig. 5

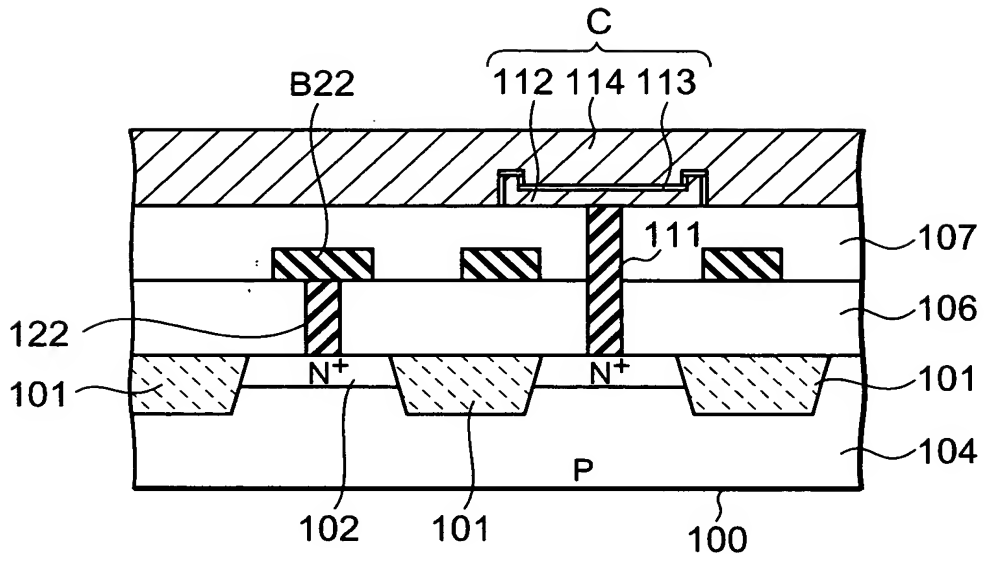


Fig. 6A

ROW ADDRESS SIGNAL XAdd	COLUMN ADDRESS SIGNAL YAdd	SELECTED MEMORY CELL	SELECTED WORD LINE	SELECTED BIT LINE
＊＊＊＊0	＊＊＊＊＊	MN-2	W11	B12
＊＊＊＊1	＊＊＊＊＊	MN	W12	B12
＊＊＊＊0	＊＊＊＊＊	MN+1	W13	B12

Fig. 6B

ROW ADDRESS SIGNAL XAdd	COLUMN ADDRESS SIGNAL YAdd	SELECTED MEMORY CELL	SELECTED WORD LINE	SELECTED BIT LINE
＊＊＊＊0	＊＊＊＊0	MN-2	W21	B22
＊＊＊＊1	＊＊＊＊1	MN	W22	B23
＊＊＊＊0	＊＊＊＊0	MN+1	W23	B22

Fig. 7

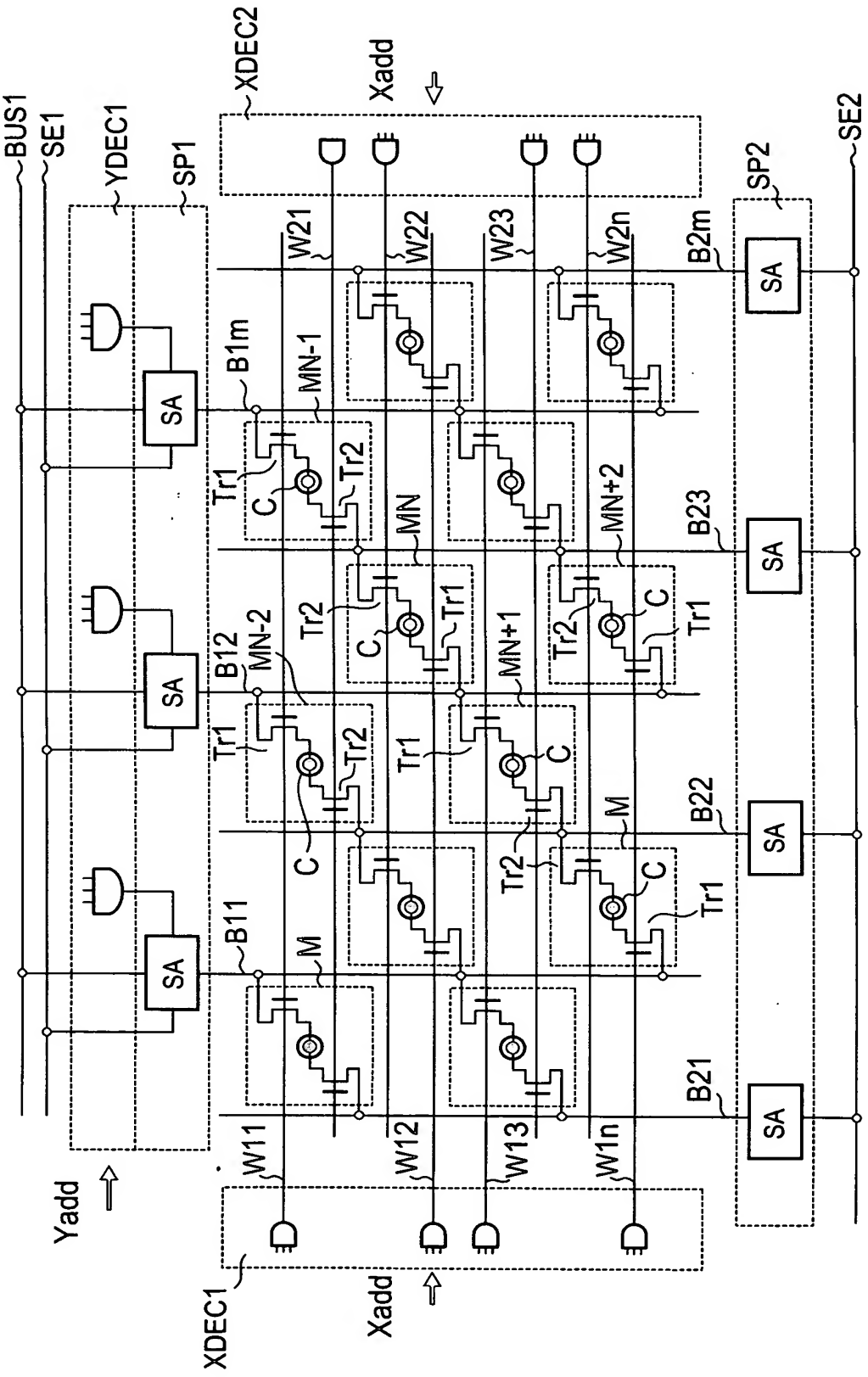

BUS1
SE1
YDEC1
SP1
XDEC2
Xadd
SP2
SE2
SA
B1m
B2m
B12
B23
B11
B22
B21
W21
W22
W23
W2n
W11
W12
W13
W1n
MN-1
MN
MN-2
MN+1
MN+2
M
Tr1
Tr2
C
Yadd
XDEC1
Xadd

Fig. 8

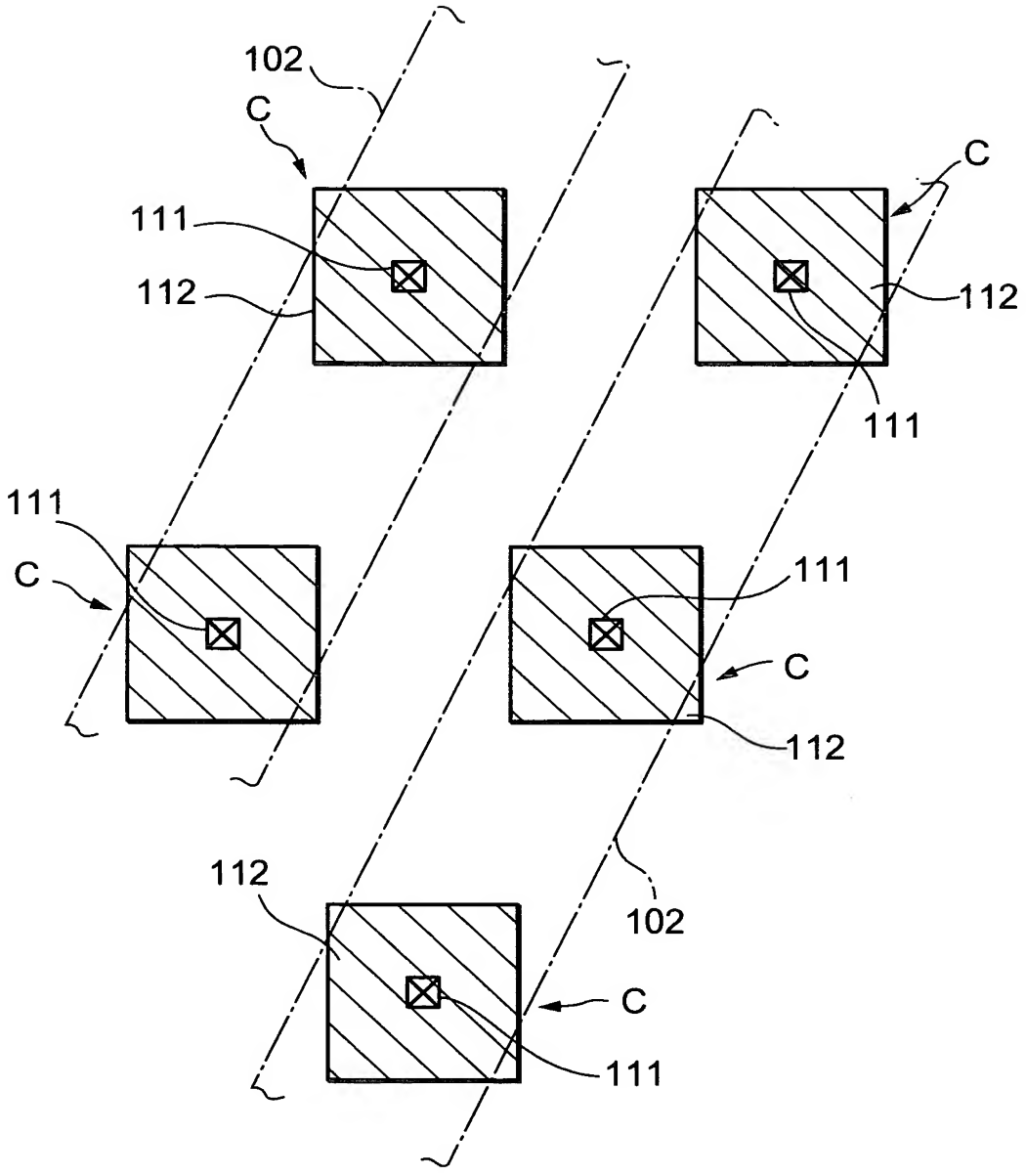


Fig. 9

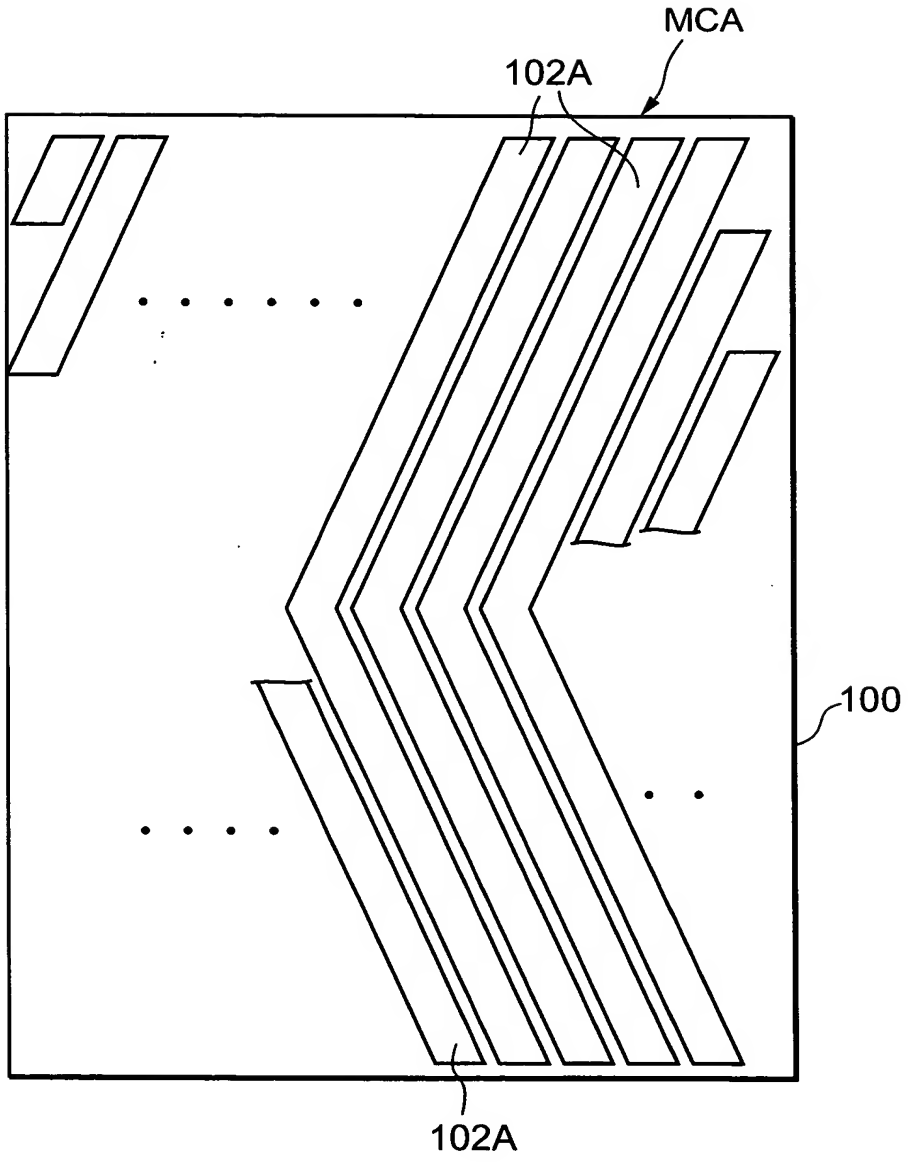


Fig. 10

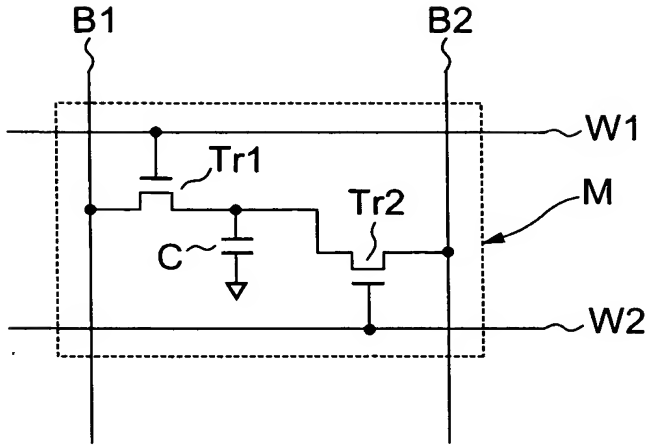
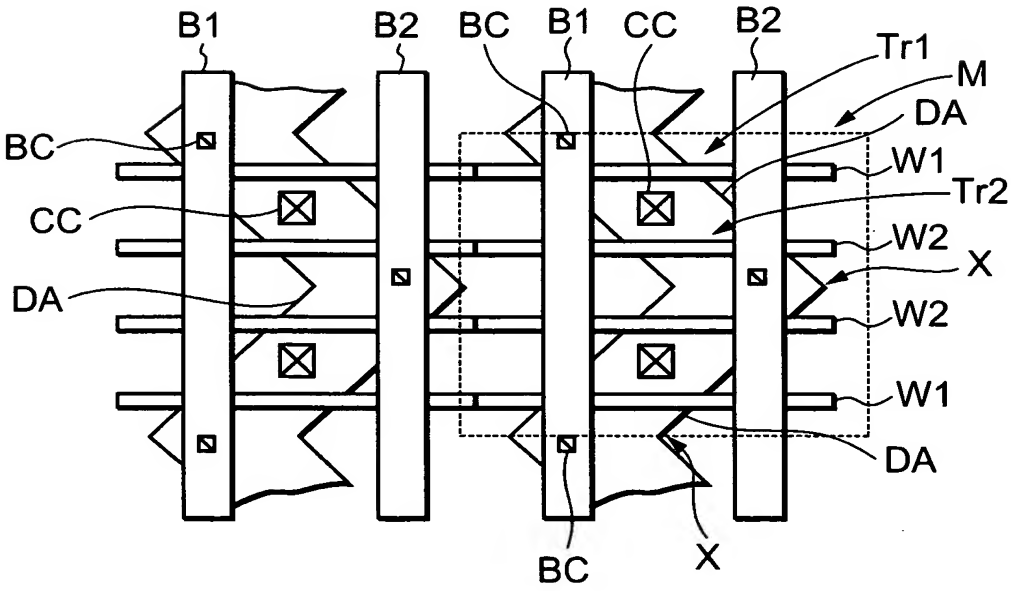

B1
B2
W1
Tr1
Tr2
M
C
W2

Fig. 11


B1
B2
BC
B1
CC
B2
Tr1
M
DA
W1
Tr2
W2
X
W2
W1
DA
BC
X
BC
CC
DA